



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/557,164	04/25/2000	William J. Dally	2789.2004-001	9280
21005	7590	03/01/2005		
HAMILTON, BROOK, SMITH & REYNOLDS, P.C. 530 VIRGINIA ROAD P.O. BOX 9133 CONCORD, MA 01742-9133			EXAMINER BAYARD, EMMANUEL	
			ART UNIT 2631	PAPER NUMBER

DATE MAILED: 03/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/557,164

Applicant(s)

DALLY ET AL.

Examiner

Emmanuel Bayard

Art Unit

2631

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 22 November 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-66 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-66 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

This is in response to amendment filed on 11/22/04 in which claims 1-66 are pending. The applicant's arguments have been fully considered but they are not persuasive enough. Therefore this case is made final. (see Examiner response to arguments below).

#### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 3718 of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-4, 7-8, 11, 18-20, 23, 24, 33-36, 39-40, 43, 50-52, 55-56, 65-66 are rejected under 35 U.S.C. 102(e) as being anticipated by Takada et al U.S. Patent No 6,246,271 B1

Art Unit: 2631

As per claims 1, 33 and 65 Takada et al teaches a data transmitter comprising: a data input (see fig. 6 element 602); plural delay elements applying different delays to the data input in parallel to provide plural delayed data signals (see figs. 2, 7 elements 11, 13 and col.2, lines 1- 65 and col.3, lines 42-67 and col.6, lines 46-67); an adder is the same as the claimed (data output combining) the delayed data signals (see figs. 2, 7 element 14 and col.2, lines 13-17, 48-50 and col.3, lines 55-56), a control signal is the same as the claimed (transition time) (see figs. 2, 7 and col.3, line 53 and col.4, line 26) of the data output being determined by difference in delays applied to the data input.

As per claims 2, 34 the data transmitter of Takada et al does include parallel delay connection (see figs. 2, 7).

As per claims 3, 35 the data transmitter of Takada et al teaches a frequency multiplier for use in a clock generator (see col.1, lines 15-17). Therefore a clock signal applied the delay elements and different delays and applied to the data input is inherently included in Takada.

As per claims 4, 8, 20, 24, 36, 40, 52 and 56, the data transmitter of Takada et al includes a plural driver circuits (see col4, lines 63-67).

As per claims 7, 39 the data transmitter of Takada et al includes parallel data input (see figs. 2, 7).

As per claims 11, 43, the data transmitter of Takada et al inherently includes data output is proportional to bit time.

As per claims 18, 50 and 66, Takada et al teaches a data transmitter comprising: a data input (see figs. 2, 7 element Fin1); Takada a frequency

Art Unit: 2631

multiplier for use in a clock generator (see col.1, lines 15-17) therefore a bit clock is inherently included in Takada; a control signal is the same as the claimed (transition time control) (see figs. 2, 7 and col.3,line 53 and col.4, line 26) for receiving the data input and providing a controlled data signal, the transition time control controlling the transition time of the controlled signal to be proportional to bit time of the bit clock (see col.1, lines 15-17 ) . When the delay stage is enable a clock signal will pass therefore generating a time period which is considered as the claimed (the transition time control controlling the transition time of the controlled signal to be proportional to bit time of the bit clock).

As per claims 19 and 51, the data transmitter of Takada et al teaches a frequency multiplier for use in a clock generator (see col.1, lines 15-17).

Therefore a clock signal applied the delay elements and different delays and applied to the data input is inherently included in Takada.

As per claims 23 and 55 the data transmitter of Takada et al does include parallel data input (see figs. 2, 7).

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2631

4. Claims 5-6, 9-10, 12-17, 21-22, 25-32, 37-38, 41-42, 44-49, 53-54, 57-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over of Takada et al U.S. Patent No 6,246,271 B1 in view of Bae U.S. Patent No 6,242,960 B1.

As per claims 5, 9, 21, 25, 37, 41, 53 and 57 Harvey et al disclose all the features of the claimed invention except each delay having CMOS invertors.

Bae teaches delay having CMOS invertors (see fig.1 elements 146-158 and col.3, lines 17-18, 45-48).

It would have been obvious to one skill in the art to incorporate the CMOS invertors of Bae into of Takada et al as to invert the phase of the reference clock signal as taught by Bae (see col.3, lines 36-37).

As per claims 6, 10, 22, 26, 38, 42, 54 and 58, the transmitter of Bae does include a loading device, which is functionally equivalent to the claimed (load capacitance) (see col.4, lines 47-60). Furthermore implementing such loading into of Takada et al would have been obvious to one of ordinary skill in the art as to control the provided power supply into the transistors.

As per claims 13, 16, 28, 31, 45, 48, 60, 63 of Takada et al discloses a circuit to control power supply voltage to the delay elements, the circuit comprising: a first and second delay elements, each receiving a common clock signal and a phase comparator (see fig.1 element 103) which compares the outputs of the first and second delay elements and control a supply voltage applied to the first and second delay elements to control phase difference of the outputs (see col.4, lines 13-67 and col.7, lines 13-20).

Art Unit: 2631

As per claims 12, 15, 27, 30, 44, 47, 59, 62, the circuit of Takada et al does include a supply voltage (see fig.3 elements Vdd and col.4, lines 17-67) to control the delay elements.

As per claims 14, 17, 29, 32, 46, 49, 61 and 64, the transmitter of Takada et al does include a first and second delay elements having a sequence of n elements and a clock signal frequency (see figs. 2, 7).

### ***Response to Arguments***

1. Applicant's arguments filed 11/22/04 have been fully considered but they are not persuasive.

In page 2 of the response, applicant argues that Takada does not teach a rising time or falling time of the data output. However examiner respectfully disagrees.

In fact the Tadaka reference clearly teaches a process of determining the rise of fall of the data signal (see abstract and col.2, lines 25-50 and col.4, lines 58=67 and col.5, lines 1-67). By determining the rise or fall or High of Low of the data signal, Tadaka inherently teaches the change in time at each state during the transition. Therefore applicant's arguments are moot and this case is made final.

### ***Conclusion***

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is

Art Unit: 2631

filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.


Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Art Unit: 2631

Emmanuel Bayard  
Primary Examiner  
Art Unit 2631

2/24/05



EMMANUEL BAYARD  
PRIMARY EXAMINER